ABSTRACT OF THE DISCLOSURE

Semiconductor processing methods of forming conductive projections and methods of increasing alignment tolerances are described. In one implementation, a conductive projection is formed over a substrate surface area and includes an upper surface and a side surface joined therewith to define a corner region. The corner region of the conductive projection is subsequently beveled to increase an alignment tolerance relative thereto. In another implementation, a conductive plug is formed over a substrate node location between a pair of conductive lines and has an uppermost surface. Material of the conductive plug is unevenly removed to define a second uppermost surface, at least a portion of which is disposed elevationally higher than a conductive line. In one aspect, conductive plug material can be removed by facet etching the conductive plug. In another aspect, conductive plug material is unevenly doped with dopant, and conductive plug material containing greater concentrations of dopant is etched at a greater rate than plug material containing lower concentrations of dopant.